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EXAMINER	
THANGAVELU, KANDASAMY	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 01/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,198	GAUTHIER ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communicati n appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *September 30, 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to the Applicants' amendment dated September 30, 2004. Claims 1-13 of the application are pending in the application. This office action is made non-final.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. §112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

3.1 Claim 1 states, "An apparatus for modeling an anti-resonance circuit of a microprocessor, comprising:

a load model that simulates the anti-resonance circuit;

a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model".

Claim 2 states, " The apparatus of claim 1, wherein the load model simulates the anti-resonance circuit with a resistor".

1. Does this mean that the apparatus is used for modeling the anti-resonance circuit and simulating the anti-resonance circuit? If so, why does the preamble of claim 1 state that the apparatus is for modeling the anti-resonance circuit only?

2. The apparatus consists of one resistor, one transistor and one capacitor. If so, does the apparatus consist of only hardware elements and therefore is a hardware model? Should it be more appropriately called an emulator? But the claim limitations state that the resistor simulates anti-resonance circuit; the transistor simulates one high frequency capacitor and the capacitor simulates an intrinsic capacitance of a section of the microprocessor. Does this mean that simulation is done using mathematical models of anti-resonance circuit, high frequency capacitor and an intrinsic capacitance of a section of the microprocessor? If not, does the simulation use mathematical models of a resistor, a transistor and a capacitor? Are the mathematical models converted into software simulation models and simulation done using the software simulation model? The specification does not specify if the model is made up of only hardware elements or if it is a software simulation model.

3. Claims 1 and 2 state that the resistor, the transistor and the capacitor simulate the anti-resonance circuit, a high frequency capacitor and an intrinsic capacitance of a section of the microprocessor. Claim 4 states that the load model simulates the anti-resonance circuit in

synchronization with a clock cycle. Claim 6 states that the load model begins to simulate the anti-resonance circuit on the leading edge of the clock cycle. So a clock cycle is applied to the resistor at the leading edge of the clock cycle. Does that mean that the clock cycle is then immediately removed from the resistor simulating the anti-resonance circuit? What are the outputs measured by the simulator? How are the outputs measured and recorded? Are the outputs displayed by the simulation process for evaluating the performance of the anti-resonance circuit? How is the simulation process controlled and executed? How is the simulation used to improve the design of the chip or its power system? What design parameters are changed as a result of analysis of the simulation results?

4. Specification Page 3, Para 0007 states, "actively increasing the voltage variations across their terminals with added on-chip decoupling capacitance. Figure 4 shows a schematic of this technique with resistance losses". Amended Para 0009 states, "Figure 5a shows a schematic 44 of an implementation of the method of Figure 4". Does this mean that the anti-resonance circuit is used as a replacement of the decoupling capacitor?

5. Where are the anti-resonance circuits located in a microprocessor and how many anti-resonance circuits are used in a microprocessor? Is the number of anti-resonance circuits used in the microprocessor same as the number of decoupling capacitors that would be used in the microprocessor? Figure 2 of the Herrell reference shows the decoupling capacitors are used in the microprocessor system on the chip, on the board and on the package. Does that mean that the anti-resonance circuits are also used on the chip, on the board and on the package? Specification Page 4, Para 0012 states, "a model of the package/chip anti-resonance circuit".

Does that mean only one anti-resonance circuit is used and it is located between the package and chip of Figure 6.

6. Specification Page 7, Para 0032 states, "a model of the power distribution system of a chip... the connection from the package via 72 is split into parallel paths that connect to nine separate models76a-76i for the bump and grid components of the chip .. each of the bump and grid components 76a-76i is then connected by a via 78a-78i to a designated chip section model. Fig 7b shows the block diagram 79 of an inter-connecting grid of the nine section models 80a-80i...". Therefore, the chip is represented by nine section models. Specification Page 8, Para 0034 states, "Figure 8 shows a schematic 84 of a circuit model of a section model ... the section model, in general represents a physical section of the chip... the model includes a load 86 that is connected to a transistor .. and a voltage controlled resistor.. ". Para 0035 states, "Figure 9 shows a schematic of a circuit model of a load of chip. The load includes the representation of the anti-resonance circuit of the package/chip interconnection". Does this mean that there are nine anti-resonance circuits in the model, one corresponding to each section model?

7. Specification Page 8, Para 0034 sates, "the load 86 represents a load model for that section of the chip". Para 0035 states, "The load includes the representation of the anti-resonance circuit of the package/chip interconnection". So this mean the load includes the load for that section of the chip and the load for the anti-resonance circuit of the package/chip interconnection. If so, what part of the load represents the section of the chip and what part represents the anti-resonance circuit in Figure 8? How does one determine what part of the load simulates the anti-resonance circuit of the package/chip interconnection? What procedure or algorithm is used to select a part of the load to represent the section of the chip and a part of the

load to represent the ant-resonance circuit? Since the load actually simulates a section of the chip and an anti-resonance circuit, how does the designer obtain the simulation results for the anti-resonance circuit from the combined simulation of the chip section and the anti-resonance circuit?

8. Specification Page 8, Para 0034 states, "circuit model of a section model ... the section model represents a physical section of a chip. The model includes a load 86 that is connected to a transistor and a voltage controlled capacitor ... the load represents a load model for that section of the chip ...". Para 0035 states, " circuit model of a load of a chip. The load includes the representation of the anti-resonance circuit of the package/chip interconnection".

Since a section model simulates only one section of the chip and its associated anti-resonance circuit of the package/chip interconnection, does the simulation model use simultaneously nine section models and models of nine anti-resonance circuits to simulate the microprocessor and its power system? If so, should the apparatus comprise of nine section models each comprising a load model, a transistor and a capacitor? Since claim 1 states only one anti-resonance circuit, what happens to the remaining eight section models and their associated anti-resonance circuits, resistors, transistors and capacitors? If the apparatus is used to simulate only one anti-resonance circuit, how are the interfaces and interactions of this one anti-resonance circuit with other section models and the anti-resonance circuits incorporated in the simulation? Figure 7B shows the interconnection of each section model with other section models through channels indicating their interaction between section models and this needs to be included in the simulation.

9. Claim 1 states, "a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model". Specification Page 8, Para 0034 states, "the transistor represents the local high frequency capacitors". The specification does not describe the high frequency capacitors anywhere else. Where are the high frequency capacitors located and for what purpose?

10. Why is the anti-resonance circuit simulated with a section model of the microprocessor and its associated high frequency capacitor model and the intrinsic capacitance of the section?

11. Claim 4 states, "the load model simulates the anti-resonance circuit in synchronization with a clock cycle". Claim 6 states, "the load model begins to simulate the anti-resonance circuit on a leading edge of the clock cycle". What does this mean? The clock cycles are produced by the CPU clock and are applied to the model of the anti-resonance circuit. However, what is synchronization and how is it achieved? Does this mean that the clock cycles are applied to the model of the anti-resonance circuit only at the time of the leading edge of the clock cycle? Is the clock cycle cut-off immediately after application to the anti-resonance circuit? What is done to synchronize the simulation with the leading edge of the clock cycle?

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

4. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled

in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 7 states, " An apparatus for modeling an anti-resonance circuit of a microprocessor, comprising:

means for simulating an anti-resonance circuit; and

means for synchronizing the means for simulating an anti-resonance circuit with a clock signal".

However, the apparatus for modeling the anti-resonance circuit, the means for simulating the anti-resonance circuit and the means for synchronizing the means for simulating the anti-resonance circuit are not described in the specification in sufficient detail to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention as explained in paragraph 3.1 above.

5. Claims 8-13 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 8-13 are the method claims having the same limitations as the apparatus claims 1-6. They raise the same issues as claims 1-6 as explained in Paragraph 3.1 above. They are rejected for the same reasons as claims 1-6, as explained in Paragraph 3.1 above.

6. Claims 1-6 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

6.1 Claim 1 states, "An apparatus for modeling an anti-resonance circuit of a microprocessor, comprising:

a load model that simulates the anti-resonance circuit;

a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model".

Claim 2 states, " The apparatus of claim 1, wherein the load model simulates the anti-resonance circuit with a resistor".

1. Does this mean that the apparatus is used for modeling the anti-resonance circuit and simulating the anti-resonance circuit? If so, why does the preamble of claim 1 state that the apparatus is for modeling the anti-resonance circuit only?

2. The apparatus consists of one resistor, one transistor and one capacitor. If so, does the apparatus consist of only hardware elements and therefore is a hardware model? Should it be more appropriately called an emulator? But the claim limitations state that the resistor simulates anti-resonance circuit; the transistor simulates one high frequency capacitor and the capacitor simulates an intrinsic capacitance of a section of the microprocessor. Does this mean that simulation is done using mathematical models of anti-resonance circuit, high frequency capacitor and an intrinsic capacitance of a section of the microprocessor? If not, does the simulation use mathematical models of a resistor, a transistor and a capacitor? Are the mathematical models converted into software simulation models and simulation done using the software simulation model? The specification does not specify if the model is made up of only hardware elements or if it is a software simulation model.

3. Claims 1 and 2 state that the resistor, the transistor and the capacitor simulate the anti-resonance circuit, a high frequency capacitor and an intrinsic capacitance of a section of the microprocessor. Claim 4 states that the load model simulates the anti-resonance circuit in synchronization with a clock cycle. Claim 6 states that the load model begins to simulate the anti-resonance circuit on the leading edge of the clock cycle. So a clock cycle is applied to the resistor at the leading edge of the clock cycle. Does that mean that the clock cycle is then immediately removed from the resistor simulating the anti-resonance circuit? What are the outputs measured by the simulator? How are the outputs measured and recorded? Are the outputs displayed by the simulation process for evaluating the performance of the anti-resonance circuit? How is the simulation process controlled and executed? How is the simulation used to

improve the design of the chip or its power system? What design parameters are changed as a result of analysis of the simulation results?

4. Specification Page 3, Para 0007 states, "actively increasing the voltage variations across their terminals with added on-chip decoupling capacitance. Figure 4 shows a schematic of this technique with resistance losses". Amended Para 0009 states, "Figure 5a shows a schematic 44 of an implementation of the method of Figure 4". Does this mean that the anti-resonance circuit is used as a replacement of the decoupling capacitor?

5. Where are the anti-resonance circuits located in a microprocessor and how many anti-resonance circuits are used in a microprocessor? Is the number of anti-resonance circuits used in the microprocessor same as the number of decoupling capacitors that would be used in the microprocessor? Figure 2 of the Herrell reference shows the decoupling capacitors are used in the microprocessor system on the chip, on the board and on the package. Does that mean that the anti-resonance circuits are also used on the chip, on the board and on the package? Specification Page 4, Para 0012 states, "a model of the package/chip anti-resonance circuit". Does that mean only one anti-resonance circuit is used and it is located between the package and chip of Figure 6.

6. Specification Page 7, Para 0032 states, "a model of the power distribution system of a chip... the connection from the package via 72 is split into parallel paths that connect to nine separate models76a-76i for the bump and grid components of the chip .. each of the bump and grid components 76a-76i is then connected by a via 78a-78i to a designated chip section model. Fig 7b shows the block diagram 79 of an inter-connecting grid of the nine section models 80a-80i...". Therefore, the chip is represented by nine section models. Specification Page 8, Para

0034 states, "Figure 8 shows a schematic 84 of a circuit model of a section model ... the section model, in general represents a physical section of the chip... the model includes a load 86 that is connected to a transistor .. and a voltage controlled resistor.. ". Para 0035 states, "Figure 9 shows a schematic of a circuit model of a load of chip. The load includes the representation of the anti-resonance circuit of the package/chip interconnection". Does this mean that there are nine anti-resonance circuits in the model, one corresponding to each section model?

7. Specification Page 8, Para 0034 sates, "the load 86 represents a load model for that section of the chip". Para 0035 states, "The load includes the representation of the anti-resonance circuit of the package/chip interconnection". So this mean the load includes the load for that section of the chip and the load for the anti-resonance circuit of the package/chip interconnection. If so, what part of the load represents the section of the chip and what part represents the anti-resonance circuit in Figure 8? How does one determine what part of the load simulates the anti-resonance circuit of the package/chip interconnection? What procedure or algorithm is used to select a part of the load to represent the section of the chip and a part of the load to represent the ant-resonance circuit? Since the load actually simulates a section of the chip and an anti-resonance circuit, how does the designer obtain the simulation results for the anti-resonance circuit from the combined simulation of the chip section and the anti-resonance circuit?

8. Specification Page 8, Para 0034 states, "circuit model of a section model ... the section model represents a physical section of a chip. The model includes a load 86 that is connected to a transistor and a voltage controlled capacitor ... the load represents a load model

for that section of the chip ...". Para 0035 states, " c circuit model of a load of a chip. The load includes the representation of the anti-resonance circuit of the package/chip interconnection".

Since a section model simulates only one section of the chip and its associated anti-resonance circuit of the package/chip interconnection, does the simulation model use simultaneously nine section models and models of nine anti-resonance circuits to simulate the microprocessor and its power system? If so, should the apparatus comprise of nine section models each comprising a load model, a transistor and a capacitor? Since claim 1 states only one anti-resonance circuit, what happens to the remaining eight section models and their associated anti-resonance circuits, resistors, transistors and capacitors? If the apparatus is used to simulate only one anti-resonance circuit, how are the interfaces and interactions of this one anti-resonance circuit with other section models and the anti-resonance circuits incorporated in the simulation? Figure 7B shows the interconnection of each section model with other section models through channels indicating their interaction between section models and this needs to be included in the simulation.

9. Claim 1 states, "a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model". Specification Page 8, Para 0034 states, "the transistor represents the local high frequency capacitors". The specification does not describe the high frequency capacitors anywhere else. Where are the high frequency capacitors located and for what purpose?

10. Why is the anti-resonance circuit simulated with a section model of the microprocessor and its associated high frequency capacitor model and the intrinsic capacitance of the section?

11. Claim 4 states, "the load model simulates the anti-resonance circuit in synchronization with a clock cycle". Claim 6 states, "the load model begins to simulate the anti-resonance circuit on a leading edge of the clock cycle". What does this mean? The clock cycles are produced by the CPU clock and are applied to the model of the anti-resonance circuit. However, what is synchronization and how is it achieved? Does this mean that the clock cycles are applied to the model of the anti-resonance circuit only at the time of the leading edge of the clock cycle? Is the clock cycle cut-off immediately after application to the anti-resonance circuit? What is done to synchronize the simulation with the leading edge of the clock cycle?

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

7. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 7 states, " An apparatus for modeling an anti-resonance circuit of a microprocessor, comprising:

means for simulating an anti-resonance circuit; and

means for synchronizing the means for simulating an anti-resonance circuit with a clock signal".

However, the apparatus for modeling the anti-resonance circuit, the means for simulating the anti-resonance circuit and the means for synchronizing the means for simulating the anti-resonance circuit are not described in the specification in sufficient detail in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention as explained in paragraph 6.1 above.

8. Claims 8-13 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claims 8-13 are method claims having the same limitations as the apparatus claims 1-6. They raise the same issues as claims 1-6 as explained in Paragraph 6.1 above. They are rejected for the same reasons as claims 1-6, as explained in Paragraph 6.1 above.

9. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

1. Claim 1 states, "an apparatus for modeling an anti-resonance circuit of a microprocessor". However, it includes a load model that simulates the anti-resonance circuit, a transistor that simulates the high frequency capacitor and a capacitor that simulates an intrinsic capacitance of a section of the microprocessor. Therefore, it is not clear if the apparatus is a modeling tool or a modeling and simulating tool and so the apparatus is vague and indefinite.

2. The apparatus consists of one resistor, one transistor and one capacitor. If so, it is vague and indefinite if the apparatus consists of only hardware elements and therefore is a hardware model. The claim limitations state that the resistor simulates anti-resonance circuit; the transistor simulates one high frequency capacitor and the capacitor simulates an intrinsic capacitance of a section of the microprocessor. It is vague and indefinite if the simulation is done using mathematical models of anti-resonance circuit, high frequency capacitor and an intrinsic capacitance of a section of the microprocessor or the simulation uses mathematical models of a resistor, a transistor and a capacitor. The specification does not specify if the model is made up of only hardware elements or if it is a software simulation model.

3. Specification Page 8, Para 0034 sates, "the load 86 represents a load model for that section of the chip". Para 0035 states, "The load includes the representation of the anti-resonance circuit of the package/chip interconnection". So this mean the load includes the load for that section of the chip and the load for the anti-resonance circuit of the package/chip interconnection. It is vague and indefinite as to what part of the load represents the section of the chip and what part represents the anti-resonance circuit

Claims rejected but not specifically addressed are rejected based on their dependency on rejected claims.

11. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 states, " An apparatus for modeling an anti-resonance circuit of a microprocessor, comprising:

means for simulating an anti-resonance circuit; and

means for synchronizing the means for simulating an anti-resonance circuit with a clock signal".

1. Claim 7 states, "an apparatus for modeling an anti-resonance circuit of a microprocessor". However, it includes means for simulating an anti-resonance circuit, and means for synchronizing the means for simulating an anti-resonance circuit. Therefore, it is not clear if the apparatus is a modeling tool or a modeling and simulating tool and so the apparatus is vague and indefinite.

2. The means for simulating an anti-resonance circuit, and the means for synchronizing the means for simulating the anti-resonance circuit are not described in the specification in sufficient detail as explained in Paragraph 3.1 above. Therefore the means for

simulating the anti-resonance circuit and the means for synchronizing the anti-resonance circuit are vague and indefinite.

12. Claims 8-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 8-13 are method claims having the same limitations as the apparatus claims 1-6. They raise the same issues as claims 1-6 as explained in Paragraph 10.1 above. They are rejected for the same reasons as claims 1-6, as explained in Paragraph 10.1 above.

13. Claim 1 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are:

Claim 1 states "an apparatus for modeling an anti-resonance circuit of a microprocessor". However, the claim limitations list simulating an anti-resonance circuit, simulating at least one high frequency capacitor and simulating an intrinsic capacitance of a section of the microprocessor. So simulation is performed using this apparatus.

If so, the apparatus requires a computer with a processor and memory to perform the simulation. It should also include a recording means for recording the outputs of the simulator. It may also require a means for displaying the outputs of the simulation process for evaluating the

performance of the anti-resonance circuit. Means for controlling the simulation process may also be required. Means for using the simulation to improve the design of the chip or its power system may also be included.

14. Claim 7 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential structural cooperative elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are:

Claim 7 states "an apparatus for modeling an anti-resonance circuit of a microprocessor". However, the claim limitations list means for simulating an anti-resonance circuit and means for synchronizing the means for simulating an anti-resonance circuit. So simulation is performed using this apparatus.

If so, the apparatus requires a computer with a processor and memory to perform the simulation. It should also include a recording means for recording the outputs of the simulator. It may also require a means for displaying the outputs of the simulation process for evaluating the performance of the anti-resonance circuit. Means for controlling the simulation process may also be required. Means for using the simulation to improve the design of the chip or its power system may also be included.

15. Claim 8 is rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are:

Claim 8 states "method for modeling an anti-resonance circuit of a microprocessor". However, the claim limitations list simulating an anti-resonance circuit, simulating at least one high frequency capacitor and simulating an intrinsic capacitance of a section of the microprocessor. So simulation is performed using this apparatus.

If so, the method requires storing a program representing the simulation model in a computer memory and executing the program using the processor in the computer to perform the simulation. It should also include a step for recording the outputs of the simulator. It may also require a step for displaying the outputs of the simulation process for evaluating the performance of the anti-resonance circuit. Steps for controlling the simulation process may also be required. Steps for using the simulation to improve the design of the chip or its power system may also be included.

Claim Rejections - 35 USC § 101

16. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

17. Claims 1-7 are rejected under 35 U.S.C. 101 because the claimed inventions are directed to non-statutory subject matter.

17.1 Independent claim 1 recites an apparatus for modeling an anti-resonance circuit of a

microprocessor. The limitations recited in claim contain logic elements suggesting only software components which are not statutory subject matter. To be statutory, the system should include computer system hardware components which will be required to implement the software components.

Dependent claims 2-6 depend on Claim 1 but contain logic elements suggesting only software components which do not add further statutory steps.

17.2 Independent claim 7 recites an apparatus for modeling an anti-resonance circuit of a microprocessor. The limitations recited in claim contain logic elements suggesting only software components which are not statutory subject matter. To be statutory, the system should include computer system hardware components which will be required to implement the software components.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

19. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

20. Claims 1, 2, 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Ogawa et al.** (U.S. Patent Application 2002/0011885) and **Herrell et al.** ("Modeling of power distribution systems for high-performance microprocessors", IEEE 1999).

21.1 **Larsson** teaches Resonance and damping in CMOS circuits with on-chip decoupling capacitance. Specifically, as per claim 1, **Larsson** teaches an apparatus for modeling a resonance circuit of a microprocessor (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach an apparatus for modeling an anti-resonance circuit of a microprocessor. **Evans** teaches an anti-resonance mixing filter implemented using analog components (CL1, L47-51; Fig 1, Fig 2 and Fig 3; CL2, L8-16; CL2, L65 to CL3, L10; CL3,

L16-30), as the anti-resonance circuit isolates the oscillations that are amplified when operating at resonant frequencies (CL1, L47-49). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** including an apparatus for modeling a resonance circuit of a microprocessor with the apparatus of **Evans** that included an anti-resonance mixing filter circuit. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and the anti-resonance circuit would isolate the oscillations that would be amplified when operating at resonant frequencies.

Larsson does not expressly teach an apparatus for modeling an anti-resonance circuit of a microprocessor. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

Larsson teaches a load model that simulates the resonance circuit (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2;

Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach a load model that simulates the anti-resonance circuit. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that included a load model that simulates the resonance circuit with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

Larsson does not expressly teach a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model. **Ogawa et al.** teaches a transistor that simulates at least one high frequency capacitor (Fig 1; Page 1, Para 0001, L10-14; Page 1, Para 0007, L1-12; Page 23, Para 0229), as that allows internal circuit configurations of LSI circuit to be accurately simulated with transistor models, interconnected resistance models and capacitance models (Page 1, Para 0007, L7-12); and the transistor description of the LSI model reduces the number of transistors constituting the model (Page 4, Para 0049, L5-7). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that with the apparatus of **Ogawa et al.** that included a transistor that simulated at least one high frequency capacitor. The artisan

would have been motivated because that would allow internal circuit configurations of LSI circuit to be accurately simulated with transistor models, interconnected resistance models and capacitance models; and the transistor description of the LSI model would reduce the number of transistors constituting the model.

Larsson does not expressly teach that the transistor is connected in parallel with the load model. **Herrell et al.** teaches that the transistor is connected in parallel with the load model (Page 240, CL1, Para 1, L1-7; Page 240, CL2, Para 2, L1-7; Page 241, CL1, Para 2, L1-3; Page 241, CL2, Para 1, L1-4; Page 241, CL2, Fig 2), as that allows capturing the main features of the power distribution network with a simplified equivalent circuit (Page 241, CL2, Para 1, L1-4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that with the apparatus of **Herrell et al.** that included the transistor connected in parallel with the load model. The artisan would have been motivated because that would allow capturing the main features of the power distribution network with a simplified equivalent circuit.

Larsson teaches a capacitor that simulates an intrinsic capacitance of a section of the microprocessor (Page 850, Fig. 1; Page850, CL1, Para 4; Page 850, CL2, Fig 2). **Larsson** does not expressly teach a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model. **Herrell et al.** teaches that the capacitor is connected in parallel with the load model (Page 240, CL1, Para 1, L1-7; Page 240, CL2, Para 2, L1-7; Page 241, CL1, Para 2, L1-3; Page 241, CL2, Para 1, L1-4; Page 241, CL2, Fig 2), as that allows capturing the main features of the power distribution network with a simplified equivalent circuit (Page 241, CL2, Para 1, L1-4). It would have been

obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that with the apparatus of **Herrell et al.** that included the capacitor connected in parallel with the load model. The artisan would have been motivated because that would allow capturing the main features of the power distribution network with a simplified equivalent circuit.

21.2 As per claim 2, **Larsson, Evans, Jackson et al., Ogawa et al.** and **Herrell et al.** teach the apparatus of claim 1. **Larsson** teaches that the load model simulates the resonance circuit with a resistor (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach that the load model simulates the anti-resonance circuit with a resistor. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that included the load model simulating the resonance circuit with a resistor with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

21.3 As per Claims 8 and 9, these are rejected based on the same reasoning as Claims 1 and 2, supra. Claims 8 and 9 are method claims reciting the same limitations as Claims 1 and 2, as taught throughout by **Larsson, Evans, Jackson et al., Ogawa et al.** and **Herrell et al.**

22. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Ogawa et al.** (U.S. Patent Application 2002/0011885), **Herrell et al.** ("Modeling of power distribution systems for high-performance microprocessors", IEEE 1999) and **Lane** (U.S. Patent 4,459,566).

22.1 As per claim 3, **Larsson, Evans, Jackson et al., Ogawa et al.** and **Herrell et al.** teach the apparatus of claim 2. **Larsson** does not expressly teach that the resistor is a voltage controlled resistor. **Lane** teaches that the resistor is a voltage controlled resistor (CL1, L65 to CL2, L11), because as per as **Ogawa et al.** the internal impedance of the LSI circuit varies depending on the input signals and voltages at the power terminals and the variations in the internal impedance or resistance makes complicated current waveforms (Page 2, Para 0011, L1-5). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Lane** that included the resistor being a voltage controlled resistor. The artisan would have been motivated because the internal impedance of the LSI circuit would vary depending on the input signals and voltages at

the power terminals and the variations in the internal impedance or resistance would make complicated current waveforms.

22.2 As per Claim 10, it is rejected based on the same reasoning as Claim 3, supra. Claim 10 is a method claims reciting the same limitations as Claim 3, as taught throughout by **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al. and Lane.**

23. Claims 4-5 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Ogawa et al.** (U.S. Patent Application 2002/0011885), **Herrell et al.** ("Modeling of power distribution systems for high-performance microprocessors", IEEE 1999) and **Culler** (U.S. Patent 6,370,678).

23.1 As per claim 4, **Larsson, Evans, Jackson et al., Ogawa et al.** and **Herrell et al.** teach the apparatus of claim 1. **Larsson** does not expressly teach that the load model simulates the anti-resonance circuit in synchronization with a clock cycle. **Culler** teaches that the load model simulates the anti-resonance circuit in synchronization with a clock cycle (CL3, L30-42; CL4, L49-59), as that allows determining the primary resonant frequencies of the power supply circuits; the resonant frequency of the on-chip power supply circuit is used as input to the initial floor planning (CL4, L55-59) and to adjust the synthesis of the core logic circuit (Cl5, L24-35). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention

to modify the apparatus of **Larsson** with the apparatus of **Culler** that included the load model simulating the anti-resonance circuit in synchronization with a clock cycle. The artisan would have been motivated because that would allow determining the primary resonant frequencies of the power supply circuits; the resonant frequency of the on-chip power supply circuit would be used as input to the initial floor planning and to adjust the synthesis of the core logic circuit.

23.2 As per claim 5, **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al.** and **Culler** teach the apparatus of claim 4. **Larsson** does not expressly teach that the clock cycle is generated by a central processing unit clock. **Culler** teaches that the clock cycle is generated by a central processing unit clock (CL3, L30-31), as the clock cycle affects the resonant frequency of the IC package since many harmonics are present in such clock signals (CL3, L30-35); and it is necessary to determine the resonant frequency of the power circuits so they could be used as inputs to the initial floor planning (Cl4, L55-59). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Culler** that included the clock cycle generated by a central processing unit clock. The artisan would have been motivated because the clock cycle would affect the resonant frequency of the IC package since many harmonics would be present in such clock signals; and it would be necessary to determine the resonant frequency of the power circuits so they could be used as inputs to the initial floor planning.

23.3 As per Claims 11 and 12, these are rejected based on the same reasoning as Claims 4 and 5, supra. Claims 11 and 12 are method claims reciting the same limitations as Claims 4 and 5, as taught throughout by **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al.** and **Culler.**

24. Claims 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Ogawa et al.** (U.S. Patent Application 2002/0011885), **Herrell et al.** ("Modeling of power distribution systems for high-performance microprocessors", IEEE 1999), **Culler** (U.S. Patent 6,370,678) and **Kunimoto et al.** (U.S. Patent 5,223,653).

24.1 As per claim 6, **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al.** and **Culler** teach the apparatus of claim 4. **Larsson** does not expressly teach that the load model begins to simulate the anti-resonance circuit on a leading edge of the clock cycle. **Kunimoto et al.** teaches that the load model begins to simulate the anti-resonance circuit on a leading edge of the clock cycle (Fig 1; CL1, L29-37; CL5, L35-37), as the elements of the circuit are selected based on the resonance characteristics of the circuit being simulated (CL1, L29-37). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Kunimoto et al.** that included the load model beginning to simulate the anti-resonance circuit on a leading edge of the clock cycle. The artisan would have been motivated because the elements of the circuit would be selected based on the resonance characteristics of the circuit being simulated.

24.2 As per Claim 13, it is rejected based on the same reasoning as Claim 6, supra. Claim 13 is a method claims reciting the same limitations as Claim 6, as taught throughout by **Larsson, Evans, Jackson et al., Ogawa et al., Herrell et al., Culler** and **Kunimoto et al.**

25. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Larsson** ("Resonance and damping in CMOS circuits with on-chip decoupling capacitance", IEEE 1998) in view of **Evans** (U.S. Patent 6,240,246) and **Jackson et al.** (U.S. Patent 3,808,370), and further in view of **Culler** (U.S. Patent 6,370,678).

25.1 As per claim 7, **Larsson** teaches an apparatus for modeling a resonance circuit of a microprocessor (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach an apparatus for modeling an anti-resonance circuit of a microprocessor. **Evans** teaches an anti-resonance mixing filter implemented using analog components (CL1, L47-51; Fig 1, Fig 2 and Fig 3; CL2, L8-16; CL2, L65 to CL3, L10; CL3, L16-30), as the anti-resonance circuit isolates the oscillations that are amplified when operating at resonant frequencies (CL1, L47-49). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** including an apparatus for modeling a resonance circuit of a microprocessor with the apparatus of **Evans** that included an anti-resonance mixing filter circuit. The artisan would have been motivated because that would

allow modeling an anti-resonance circuit of a microprocessor and the anti-resonance circuit would isolate the oscillations that would be amplified when operating at resonant frequencies.

Larsson does not expressly teach an apparatus for modeling an anti-resonance circuit of a microprocessor. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow modeling an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

Larsson teaches means for simulating a resonance circuit (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2; Page 854, CL1, Para 3 to CL2, Para 1). **Larsson** does not expressly teach means for simulating an anti-resonance circuit. **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the

apparatus of **Larsson** that included means for simulating a resonance circuit with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer. The artisan would have been motivated because that would allow simulating an anti-resonance circuit of a microprocessor and determining the anti-resonance information of the circuit.

Larsson does not expressly teach means for synchronizing the means for simulating an anti-resonance circuit with a clock signal. **Culler** teaches means for synchronizing the means for simulating an anti-resonance circuit with a clock signal (CL3, L30-42; CL4, L49-59), as that allows determining the primary resonant frequencies of the power supply circuits; the resonant frequency of the on-chip power supply circuit is used as input to the initial floor planning (CL4, L55-59) and to adjust the synthesis of the core logic circuit (Cl5, L24-35). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** with the apparatus of **Culler** that included means for synchronizing the means for simulating an anti-resonance circuit with a clock signal. The artisan would have been motivated because that would allow determining the primary resonant frequencies of the power supply circuits; the resonant frequency of the on-chip power supply circuit would be used as input to the initial floor planning and to adjust the synthesis of the core logic circuit.

Respons to Arguments

26. Applicant's arguments filed on September 30, 2004 have been fully considered. The arguments with respect to claim rejections under 35 USC 103 (a) made on September 30, 2004 are not persuasive. Additional claim rejections under 35 USC 112 First paragraph, 35 USC 112 Second Paragraph and 35 USC 101 are included in this office action.

27. As per the applicants' arguments, the applicants' attention is requested to the corresponding claim rejections. In addition, the following explanation is provided to further explain the examiner's position.

27.1 As per the applicants' argument that "Larson does not disclose, or otherwise teach, at least (i) a load model that simulates the anti-resonance circuit;

(ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

(iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model";

"Evans does not disclose, or otherwise teach, at least (i) a load model that simulates the anti-resonance circuit;

(ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

(iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model";

"Jackson does not disclose, or otherwise teach, at least (i) a load model that simulates the anti-resonance circuit;

(ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

(iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model";

"Ogawa does not disclose, or otherwise teach, at least (i) a load model that simulates the anti-resonance circuit;

(ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

(iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model";

"Herrell does not disclose, or otherwise teach, at least (i) a load model that simulates the anti-resonance circuit;

(ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

(iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model";

"Lane does not disclose, or otherwise teach, at least (i) a load model that simulates the anti-resonance circuit;

(ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

(iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model";

"Culler does not disclose, or otherwise teach, at least (i) a load model that simulates the anti-resonance circuit;

(ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

(iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model"; and

"Kunimoto does not disclose, or otherwise teach, at least (i) a load model that simulates the anti-resonance circuit;

(ii) a transistor that simulates at least one high frequency capacitor, wherein the transistor is connected in parallel with the load model; and

(iii) a capacitor that simulates an intrinsic capacitance of a section of the microprocessor, wherein the capacitor is connected in parallel with the load model";, the Examiner takes the position that the applicants have not fully described the anti-resonance circuit and how the load model simulates the anti-resonance circuit.

As explained in Paragraph 3.1 above the applicants have not described the following:

1. If the apparatus is used for modeling the anti-resonance circuit and simulating the anti-resonance circuit.

2. Does the apparatus consist of only hardware elements and therefore is a hardware model? The claim limitations state that the resistor simulates anti-resonance circuit; the transistor simulates one high frequency capacitor and the capacitor simulates an intrinsic capacitance of a section of the microprocessor. Does this mean that simulation is done using mathematical models of anti-resonance circuit, high frequency capacitor and an intrinsic capacitance of a section of the microprocessor? If not, does the simulation use mathematical models of a resistor, a transistor and a capacitor? Are the mathematical models converted into software simulation models and simulation done using the software simulation model?

3. Claims 1 and 2 state that the resistor, the transistor and the capacitor simulate the anti-resonance circuit, a high frequency capacitor and an intrinsic capacitance of a section of the microprocessor. Claim 4 states that the load model simulates the anti-resonance circuit in synchronization with a clock cycle. Claim 6 states that the load model begins to simulate the anti-resonance circuit on the leading edge of the clock cycle. So a clock cycle is applied to the resistor at the leading edge of the clock cycle. Does that mean that the clock cycle is then immediately removed from the resistor simulating the anti-resonance circuit?

4. What are the outputs measured by the simulator? How are the outputs measured and recorded? Are the outputs displayed by the simulation process for evaluating the performance of the anti-resonance circuit? How is the simulation process controlled and executed? How is the simulation used to improve the design of the chip or its power system? What design parameters are changed as a result of analysis of the simulation results?

5. Is the anti-resonance circuit used as a replacement of the decoupling capacitor?

6. Where are the anti-resonance circuits located in a microprocessor and how many anti-resonance circuits are used in a microprocessor? Is the number of anti-resonance circuits used in the microprocessor same as the number of decoupling capacitors that would be used in the microprocessor? Or is only one anti-resonance circuit used and is it located between the package and chip of Figure 6?

7. Are there nine anti-resonance circuits in the model, one corresponding to each section model?

8. Does the load includes the load for that section of the chip and the load for the anti-resonance circuit of the package/chip interconnection. If so, what part of the load represents the section of the chip and what part represents the anti-resonance circuit in Figure 8? How does one determine what part of the load simulates the anti-resonance circuit of the package/chip interconnection? What procedure or algorithm is used to select a part of the load to represent the section of the chip and a part of the load to represent the ant-resonance circuit? Since the load actually simulates a section of the chip and an anti-resonance circuit, how does the designer obtain the simulation results for the anti-resonance circuit from the combined simulation of the chip section and the anti-resonance circuit?

9. Since a section model simulates only one section of the chip and its associated anti-resonance circuit of the package/chip interconnection, does the simulation model use simultaneously nine section models and models of nine anti-resonance circuits to simulate the microprocessor and its power system? If so, should the apparatus comprise of nine section models each comprising a load model, a transistor and a capacitor? Since claim 1 states only one anti-resonance circuit, what happens to the remaining eight section models and their associated

anti-resonance circuits, resistors, transistors and capacitors? If the apparatus is used to simulate only one anti-resonance circuit, how are the interfaces and interactions of this one anti-resonance circuit with other section models and the anti-resonance circuits incorporated in the simulation?

10. Where are the high frequency capacitors located and for what purpose?

11. Why is the anti-resonance circuit simulated with a section model of the microprocessor and its associated high frequency capacitor model and the intrinsic capacitance of the section?

12. Claim 4 states, "the load model simulates the anti-resonance circuit in synchronization with a clock cycle". Claim 6 states, "the load model begins to simulate the anti-resonance circuit on a leading edge of the clock cycle". What does this mean? The clock cycles are produced by the CPU clock and are applied to the model of the anti-resonance circuit. However, what is synchronization and how is it achieved? Does this mean that the clock cycles are applied to the model of the anti-resonance circuit only at the time of the leading edge of the clock cycle? Is the clock cycle cut-off immediately after application to the anti-resonance circuit? What is done to synchronize the simulation with the leading edge of the clock cycle?

In view of the serious deficiency in the specification and claim limitations, the Examiner has applied wide interpretation of the claim limitations in applying the prior art for art rejections.

Larsson teaches a load model that simulates the resonance circuit (Page 850, Fig. 1; Page 849, CL1, Para 1, L1-6; Page 849, CL1, Para 3, L1-2; Page 849, CL1, Para 3, L11-13; Page 849, CL2, Para 1, L2-5; Page 849, CL2, Para 2, L1-8; Page850, CL1, Para 4; Page 850, CL2, Fig 2;

Page 854, CL1, Para 3 to CL2, Para 1). **Jackson et al.** teaches an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer (CL1, L6-15; CL1, L47-51Fig 2a; CL5, L36-51), as that allows determining the anti-resonance information of the circuit (CL1, L47-51). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that included a load model that simulates the resonance circuit with the apparatus of **Jackson et al.** that included an anti-resonance mixing filter implemented using digital filter equipment consisting of delay circuits, variable amplifier circuit, fixed amplifier circuit and a summer.

Ogawa et al. teaches a transistor that simulates at least one high frequency capacitor (Fig 1; Page 1, Para 0001, L10-14; Page 1, Para 0007, L1-12; Page 23, Para 0229), as that allows internal circuit configurations of LSI circuit to be accurately simulated with transistor models, interconnected resistance models and capacitance models (Page 1, Para 0007, L7-12); and the transistor description of the LSI model reduces the number of transistors constituting the model (Page 4, Para 0049, L5-7).

Herrell et al. teaches that the transistor is connected in parallel with the load model (Page 240, CL1, Para 1, L1-7; Page 240, CL2, Para 2, L1-7; Page 241, CL1, Para 2, L1-3; Page 241, CL2, Para 1, L1-4; Page 241, CL2, Fig 2), as that allows capturing the main features of the power distribution network with a simplified equivalent circuit (Page 241, CL2, Para 1, L1-4).

Larsson teaches a capacitor that simulates an intrinsic capacitance of a section of the microprocessor (Page 850, Fig. 1; Page850, CL1, Para 4; Page 850, CL2, Fig 2). **Herrell et al.** teaches that the capacitor is connected in parallel with the load model (Page 240, CL1, Para 1,

L1-7; Page 240, CL2, Para 2, L1-7; Page 241, CL1, Para 2, L1-3; Page 241, CL2, Para 1, L1-4; Page 241, CL2, Fig 2), as that allows capturing the main features of the power distribution network with a simplified equivalent circuit (Page 241, CL2, Para 1, L1-4). It would have been obvious to one of ordinary skill in the art at the time of Applicants' invention to modify the apparatus of **Larsson** that with the apparatus of **Herrell et al.** that included the capacitor connected in parallel with the load model.

Conclusion

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska, can be reached on 571-272-3716. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K. Thangavelu
Art Unit 2123
January 8, 2005

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